**Department of Computer Engineering**

BLG 242E  
Digital Circuits Laboratory Experiment Report

Experiment : 3 Binary Arithmetic

Experiment Date : 18.03.2016

Group Number : 11

Group Members :

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# Introduction

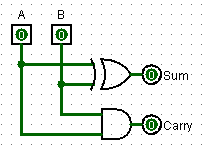
In this experiment, we implemented logic circuits for arithmetic operations on signed and unsigned binary numbers. In addition, we used the Arithmetic Logic Unit (ALU) integrated circuit to carry out basic operations.

# Arithmetic Logic Unit (ALU) integrated circuit to carry out basic operations.Requirements

## Half Adder

We implemented an XOR and an AND gate to make a half adder which adds two binary numbers and also gives their carry output.

|  |  |  |  |
| --- | --- | --- | --- |
| A | B | Sum  (A\oplusB) | Carry  (A.B) |
| 0 | 0 | 0 | 0 |
| 0 | 1 | 1 | 0 |
| 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 1 |



We implemented the circuit with:

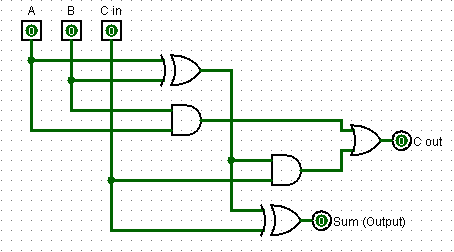
- 74xx86 - Quadruple 2-input Positive Exclusive Or (XOR) Gates

- 74xx08 - Quadruple 2-input Positive AND Gate

## Full Adder

We used the same circuit with part 1 and added an input (Cin), XOR, AND and OR gates to make a full adder.

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| A | B | Cin | Sum  (A\oplusB) | Carry  (A.B) | Sum.Cin | Output(Sum)  (Sum\oplusCin) | Cout  (Sum.Cin)+Carry |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 |
| 0 | 1 | 0 | 1 | 0 | 0 | 1 | 0 |
| 0 | 1 | 1 | 1 | 0 | 1 | 0 | 1 |
| 1 | 0 | 0 | 1 | 0 | 0 | 1 | 0 |
| 1 | 0 | 1 | 1 | 0 | 1 | 0 | 1 |
| 1 | 1 | 0 | 0 | 1 | 0 | 0 | 1 |
| 1 | 1 | 1 | 0 | 1 | 0 | 1 | 1 |



We implemented the circuit with:

- 74xx86 - Quadruple 2-input Positive Exclusive Or (XOR) Gates

- 74xx08 - Quadruple 2-input Positive AND Gate

- 74xx32 - Quadruple 2-input Positive OR Gates

# Conclusion

Comment on any difficulties you have faced, what you have learned etc.